WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising:

forming a fin structure on an insulator;

forming a gate structure over a portion of the fin structure;

forming a dielectric layer adjacent the gate structure;

removing material in the gate structure;

reducing a width of a portion of the fin structure; and

depositing a metal to replace the removed material in the gate structure.

2. The method of claim 1, wherein the forming a fin structure includes:

depositing a dielectric layer on a silicon layer, and

etching the dielectric layer and the silicon layer to define the fin structure including a silicon fin and a dielectric cap.

3. The method of claim 2, further comprising:

growing oxide layers on sides of the silicon fin.

4. The method of claim 3, further comprising, after said removing and before said reducing:

removing the oxide layers on sides of the silicon fin.

5. The method of claim 1, wherein the forming a gate structure includes:

depositing a gate material over the fin structure, and

selectively etching the gate material to define the gate structure.

6. The method of claim 1, wherein the forming a dielectric layer includes:

depositing an oxide material over the gate structure, and

polishing the oxide material until a top surface of the oxide material is coplanar with a top surface of the gate structure and the top surface of the gate structure is exposed.

7. The method of claim 1, wherein the removing material in the gate structure includes:

etching the gate structure to form a gate recess.

8. The method of claim 7, wherein the reducing includes:

reducing the width of the portion of the fin structure below the gate recess.

9. The method of claim 1, wherein the reducing includes:

reducing the width of the portion of the fin structure by about 30 nm to about 80 nm in a channel region of the semiconductor device.

10. The method of claim 1, wherein the reducing includes:

wet etching the portion of the fin structure to reduce the width.

11. The method of claim 1, further comprising:

removing the dielectric layer.

12. A method of manufacturing a semiconductor device, comprising:

forming a fin on an insulator;

forming a gate oxide on sides of the fin;

forming a gate structure over the fin and the gate oxide;

forming a dielectric layer adjacent the gate structure;

removing material in the gate structure to define a gate recess; and

reducing a width of a portion of the fin below the gate recess; and

forming a metal gate in the gate recess.

13. The method of claim 12, further comprising, after said removing and before said reducing:

removing the gate oxide on the sides of the fin.

14. The method of claim 12, wherein the reducing includes:

reducing the width of the portion of the fin by about 30 nm to about 80 nm.

15. The method of claim 12, wherein the forming includes:

forming the fin with a width between about 40 nm and about 100 nm.

16. The method of claim 15, wherein the reducing includes:

reducing the width of the portion of the fin to a width between about 10 nm and about 50 nm.

17. The method of claim 12, further comprising, before said forming a metal gate:

forming a gate dielectric on at least the sides of the fin.

18. A method of manufacturing a semiconductor device, comprising:

forming a fin on an insulator;

forming a dielectric cap over the fin;

forming gate oxide layers on opposite sides of the fin;

forming a gate structure over the fin and dielectric cap;

forming a dielectric layer adjacent the gate structure;

removing the gate structure to define a gate recess within the dielectric layer and to expose the dielectric cap and gate oxide layers;

removing the gate oxide layers from the opposite sides of the fin;

reducing a width of the fin below the gate recess; and

forming a metal gate in the gate recess.

19. The method of claim 18, wherein the reducing includes:

reducing the width of the fin below the gate recess by about 30 nm to about 80 nm.

20. The method of claim 18, wherein the forming a fin includes:

forming the fin with a width between about 40 nm and about 100 nm, and

wherein the reducing includes:

reducing the thickness of the fin below the gate recess to a width between about 10 nm and about 50 nm.